Modeling of passive elements in circuit simulation

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1 Introduction

This short paper will describe how passive elements (resistors, inductors, capacitors and voltage sources) will be modeled in the circuit simulator. The simplest of circuits will consist of only these four types of elements. However, these passive elements form the basis of circuit simulation as advanced components and machines will also be modelled using them as a foundation. The circuit solvers used by the simulator are loop analysis and nodal analysis. The background to these circuit solvers will not be presented in this paper. Instead, this paper will present the concept of how these circuit analysis techniques are implemented in the simulator. These passive circuits will be represented in the equations for loop analysis as well as nodal analysis, though as will be described, they play very different roles in these two circuit solvers. The concepts are described using sample circuits as examples.

2 Loop Analysis

Fig. 1 below is a sample circuit with passive elements to describe how loop analysis will be performed. Though it has been depicted as a simple circuit, it can be a simplified representation of a more complex circuit. For example, the ac voltage source V_{in} could be the switched output of a single-phase voltage source converter. The inductor L_1 and capacitor C could form a low pass filter to attenuate the switching frequency harmonics generated by the converter. The resistor R_L would be the load resistor. By mere inspection, it can be determined that the above circuit will

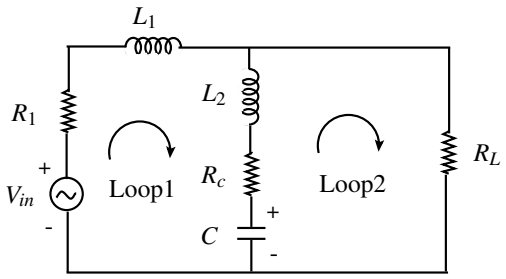

Figure 1: Sample circuit

have two independent loops. To be more precise, the above circuit has two nodes (N) and three branches (B) which implies the number of independent loops will be B-N+1=2. It can also be observed that the two independent loops can be written in two different ways. It is left to the reader to examine how another set of independent loops can be defined. With the above two loops Loop1 and Loop2, loop analysis will be performed for the circuit. To begin with the loop equations are written as follows with i_1 and i_2 being the loop currents:

$$\begin{aligned} &\text{Loop1} : V_{in} - R_1 i_1 - L_1 \frac{d}{dt} i_1 - L_2 \frac{d}{dt}(i_1 - i_2) - R_c(i_1 - i_2) - V_c = 0 \\ &\text{Loop1} : V_c - L_2 \frac{d}{dt}(i_2 - i_1) - R_c(i_2 - i_1) - R_L i_2 = 0 \end{aligned} \tag{1}$$

The above equations can be simplified further but the explanation below will describe how passive elements are included in the loop analysis.

1. Voltage Sources: The above circuit has only one voltage source V_{in}. As per Kirchoffs Voltage Law, if while progressing along the direction of the loop, the voltage source is encountered from the negative terminal to the positive terminal, then the voltage is positive in the equation. If on the other hand, the voltage source is encountered from the positive to the negative terminal while progressing along the direction of the loop, the voltage is negative in the equation. In Loop 1, Vin is encountered from the negative terminal to positive terminal and therefore is positive. On the other hand, capacitor voltage V_c is negative ($-V_c$) as capacitor is encountered from positive to negative terminal. More on the capacitor soon. Whereas in Loop 2, the capacitor is encountered from the negative to positive terminal and therefore is positive ($+V_c$).

2. Resistors: When progressing along the direction of the loop, if the voltage drop across the resistor opposes the loop current, the voltage drop is considered negative while if the voltage drop assists the loop current, the voltage drop is considered positive. Let us consider Loop 1. The voltage drop across resistor R_1 is $R_1 * i_1$. Given the direction of loop current i_1, this voltage drop will oppose i_1 and therefore is negative. Resistor R_c has current i_1-i_2 while traversing Loop 1. The voltage drop $R_c * (i_1 - i_2)$ will also oppose Loop 1 and therefore is negative. Now for Loop 2. Resistor R_c now has current $i_2 - i_1$ when traversing Loop 2 and the voltage drop $R_c * (i_2 - i_1)$ will also oppose current i_2. Therefore, the voltage drop is considered negative. In general, when a resistor is encountered, the voltage drop is determined across the resistor with respect to the loop currents that are associated with that resistor and is calculated to oppose the loop current.

3. Inductors: An inductor is very similar to the resistor except for the fact that if i is the current flowing through the inductor, $L\frac{di}{dt}$ is the voltage drop across it. In Loop 1, the voltage drop across L_1 is $L_1\frac{di_1}{dt}$. Given the direction of loop current i_1, this voltage drop will oppose i_1 and therefore is negative. Inductor L2 has current i_1-i_2 while traversing Loop 1. Therefore, the voltage drop is $L_2\frac{d(i_1-i_2)}{dt}$ and the direction will be such so as to oppose i_1. In Loop 2, the drop across L_2 as Loop 2 is traversed in the direction of i_2 is $L_2\frac{d(i_2-i_1)}{dt}$ and is such so as to oppose i_2. Therefore, in all cases, the voltage drop across in an inductor is considered negative.

4. Capacitors: A capacitor is quite different from a resistor and inductor. The voltage drop across a capacitor is $\frac{1}{C}\int idt$. Therefore, for simplicity, while representing a capacitor in loop analysis, it is considered as a voltage source V_c. This voltage source V_c is separately calculated as $\frac{1}{C}\int idt$. This can be seen in equations for Loop 1 and Loop 2. Since the capacitor is treated as a voltage source, the same rules are applied as with a voltage source. If while traversing Loop 1, the capacitor is encountered from positive terminal to negative terminal, the capacitor voltage is treated negative and vice versa. It should be noted here that the voltage of the capacitor is a function of the current through the capacitor unlike a voltage source that is independent.

The loop equations of (1) can be expressed in matrix form. It will be described how these matrices can be generated by mere observation of the circuit topology. The loop matrix equations are as follows:

$$\begin{bmatrix} L_1+L_2 & -L_2 \\ -L_2 & L_2 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} R_1+R_c & -R_c \\ -R_c & R_L+R_c \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} V_{in}-V_c \\ V_c \end{bmatrix} \tag{2}$$

Let us examine the matrices on the left hand side of the equation. First the matrices:

$$\mathbf{E} = \begin{bmatrix} L_1+L_2 & -L_2 \\ -L_2 & L_2 \end{bmatrix} \quad \text{and} \quad \mathbf{A} = \begin{bmatrix} R_1+R_c & -R_c \\ -R_c & R_L+R_c \end{bmatrix}$$

An examination of matrices **E** and **A** will show two characteristics. First, these matrices are symmetrical. Second, the diagonal elements of these matrices will never be negative. A detailed explanation is as follows.

The off-diagonal elements of the matrices are an indication of how the loops interact with each other. Examine the first KVL equation in (1). Loop 1 and Loop 2 have resistor R_c and L_2 in common. Additionally, these loops oppose each other when they pass through R_c and L_2. Therefore, the interaction between Loop 1 and Loop 2 is a $-R_c$ for **A** and $-L_2$ for **E**. Therefore, the element (1, 2) and (2, 1) of the matrix **A** is $-R_c$ and of **E** is $-L_2$. In any case, since the off-diagonal elements of matrices **A** and **E** are the interactions between the loops, these matrices will be symmetrical. However, the signs of the off-diagonal elements can be positive or negative. In the above circuit, Loop 1 and Loop 2 oppose each other over branch R_c, L_2. For this reason, all off-diagonal elements are negative. However, if the direction of Loop 2 was reversed, the elements (1, 2) and (2, 1) of matrix **A** would be $+R_c$ and of **E** would be $+L_2$. Additionally, two loops in a circuit could interact over a number of branches. In that case, the off-diagonal elements of matrices **A** and **E** will contain the sum total of the resistances and inductances of the branches. To summarize, if two loops m and n oppose each other over branches with total resistance R and total inductance L, the element (m, n) and (n, m) of matrix **A** will be -R and that of matrix **E** will be -L. Conversely, if two loops m and n assist each other over branches with total resistance R and total inductance L, the element (m, n) and (n, m) of matrix **A** will be R and that of matrix **E** will be L.

Now the second characteristic - the diagonal element will never be negative. The diagonal elements in matrices **A** and **E** are the sum total of the resistances and inductances in the loops. When applying KVL, the voltage drop across a resistance or an inductance is negative when progressing against the direction of the loop. Therefore, even for diagonal elements, one would expect a possibility of both positive and negative terms. However, let us assume that a loop is always traversed in the direction of the current indicated. Therefore, voltage drops across resistances and inductances will always be negative as per KVL. When expressed as matrix equations, the KVL equations will always result in these diagonal terms of the matrices **A** and **E** to be positive. Compare the equation (1) with (2) to understand this.

Let us now consider the right hand side of (2). The right side of the equation can be expressed by the following matrix equation:

$$\begin{bmatrix} V_{in} - V_c \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_c \end{bmatrix} = \mathbf{Bu}$$

The voltages in the KCL equation are therefore expressed as a product of an input vector **u** and the matrix **B**. The input vector **u** is merely a collection of all the voltage sources in the circuit. As stated in the description above, even capacitors are considered to be voltage sources in the KVL equation. The matrix **B** only expresses which voltages appear in a KVL equation and the direction of the voltage. For example, in the circuit above, Loop 1 has the voltage source V_{in} which is taken as positive since the loop progresses from the negative terminal to the positive terminal and element (1, 1) of matrix B is +1. The diagonal elements (1, 1) of matrix **A** and **E** are positive. However, if the direction of Loop 1 were to reversed, the loop would progress from positive terminal to negative terminal of V_{in} and therefore this source would appear as $-V_{in}$ with element (1, 1) of matrix B becoming -1. However, even in this case, element (1, 1) of matrices **A** and **E** will continue to remain positive.

To complete this section and as a precursor to the next section, let us reconsider Fig. 1 with branch directions as shown in Fig. 2. The branch directions shown by arrows are arbitrary. The direction of the arrow is towards the terminating node of the branch. As the branches are determined by the simulator, one of the nodes of a branch is the originating node and the other

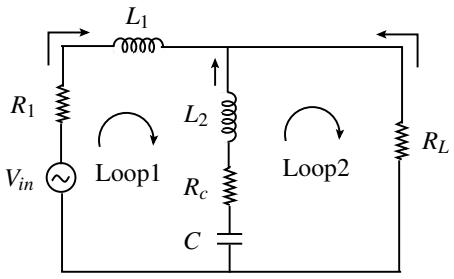

Figure 2: Sample circuit with branch directions

the terminating node. The algorithm to determine branches will not be described here, however, for any given circuit, the nodes and branches of the circuit may appear in any order. As described before, the diagonal terms of **A** and **E** will always be positive. The off-diagonal terms indicate how the loops interact with each other. Loop 1 and Loop 2 are opposing each other over the branch R_c, L_2, C with the branch being along the direction of Loop 2 and in the direction opposite to that of Loop 1. With respect to matrix **B**, Loop 1 is in the same direction as branch V_{in}, R_1, L_1 and therefore, element (1, 1) of **B** is +1 while Loop 1 is against the direction of the branch R_c, L_2, C and therefore, element (1, 2) is -1. Loop 2 has only V_c and since the branch is in the direction of the loop, element (2, 2) is +1. In this manner, an algorithm can be formulated to generate the loop analysis matrices for any circuit.

3 Nodal Analysis

This section will describe how nodal analysis will be performed on the same circuit of Figs. 1 and 2. Nodal analysis is performed by applying Kirchoff's Current Law at the nodes of the circuit. Let us again redraw the circuit in Fig. 3 to show the node voltages V_{x1} and V_{x2}. To begin with, while performing nodal analysis, one of the nodes of the circuit is chosen to be reference node and at zero potential. By observing the circuit of Fig. 3, V_{x2} would be the ideal candidate for the reference node. However, to choose a reference node in a computer program is a totally different task. Typically, any node of the circuit can be chosen to be a reference node. Therefore, randomly choosing one would not make much of a difference. Moreover, since the objective of nodal analysis is to determine currents through branches, the node voltages themselves are not

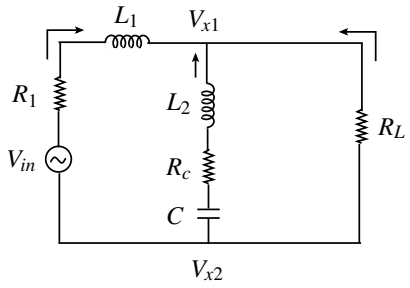

Figure 3: Sample circuit with node voltages

significant. As will described below, one of the nodes automatically becomes a reference node.

Before writing the equations, it should be described how the passive elements are modeled. The major change with respect to loop analysis is the representation of the inductors. In loop analysis, the voltage drop across the inductors are modeled as $L\frac{di}{dt}$. However, in nodal analysis, such a representation will not be convenient. If $\frac{di}{dt}$ is computed from loop analysis and used to calculate voltage drop, it is a quantity that is prone to error and noise particularly in non-linear circuits with switching converters due to the differential term. To model the inductor, we examine another quality of the inductor. The inductor will not allow the current through it to change instantaneously. Therefore, if every inductor is considered as a current source, the nodal analysis can be used to determine the node voltage and subsequently determine current flows in branches without inductors. The primary purpose of such an analysis is to determine how conduction of non-linear elements occurs when a switching takes place. In such a case, the current of the inductor freewheels through a non-linear element and therefore, considering the inductor as a current source is convenient representation. Another application of nodal analysis could be to determine the voltage across a branch that may be in a parallel with non-linear switching elements.

With the above background, the KCL equations at the two nodes can be written as follows:

$$\begin{aligned} V_{x1}: \quad & -i_{L1} - i_{L2} + \frac{V_{x1} - V_{x2}}{R_L} = 0 \\ V_{x2}: \quad & i_{L1} + i_{L2} + \frac{V_{x2} - V_{x1}}{R_L} = 0 \end{aligned} \tag{3}$$

As with the case of loop analysis, let us examine how each passive element is modeled:

1. Inductors: An inductor is modeled as a current source. The direction of current at a node

is considered positive if the direction of the branch is such that it originates at a node. On the other hand, if the branch terminates at the node, the direction of current at the node is negative.

2. Resistor: A resistor is modeled by calculating the voltage drop across it and applying it as a current. This current is considered to be flowing from the node at which the KCL equation is written to the other node of the branch. If however, an inductor is present in a branch with a resistor, the branch is treated as a current source equal to the inductor current as described above.

3. Voltage sources: A voltage source appears in the current calculated across a resistor. If a voltage source is present in a branch with a resistance, the voltage source will be negative if the positive terminal of the voltage is towards the node at which KCL is being expressed.

Since, the circuit of Fig. 3 does not consider all passive sources, let us consider Fig. 4. Another parallel branch has been added with a resistor R_f and capacitor C_f. The capacitor will be considered as a voltage source and therefore, using the capacitor it will be described how voltage sources are expressed. The nodal equations can be rewritten as:

$$\begin{aligned} V_{x1}: \quad & -i_{L1} - i_{L2} + \frac{V_{x1} - V_{x2}}{R_L} + \frac{V_{x1} - V_{cf} - V_{x2}}{R_f} = 0 \\ V_{x2}: \quad & i_{L1} + i_{L2} + \frac{V_{x2} - V_{x1}}{R_L} + \frac{V_{x2} + V_{cf} - V_{x1}}{R_f} = 0 \end{aligned} \tag{4}$$

For the KCL applied at node V_{x1}, the current through the resistor R_f is expressed across the voltage drop across it. The voltage across the branch would be the difference between the node voltages $V_{x1} - V_{x2}$. The voltage across the resistor would have to take into account the voltage across the capacitor V_{cf}. When KCL is applied at V_{x1}, the voltage V_{cf} is such that it opposes the flow of current from V_{x1} to V_{x2} since the positive terminal of capacitor C_f is towards the node V_{x1}. Therefore the voltage drop across resistor R_f is $V_{x1} - V_{cf} - V_{x2}$. On the other hand, when applying KCL at V_{x2}, the voltage drop across the resistor R_f is $V_{x2} + V_{cf} - V_{x1}$. This is because the voltage across the branch is $V_{x2} - V_{x1}$ and the voltage V_{cf} across the capacitor C_f assists the flow of current since the negative terminal of the capacitor is towards V_{x2}.

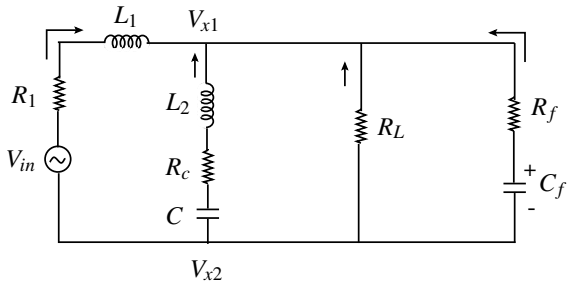

Figure 4: Sample circuit with node voltages

The nodal equations can be written in matrix form in a manner similar to the loop equations as follows:

$$\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_c \\ V_{cf} \end{bmatrix} + \begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \end{bmatrix} + \begin{bmatrix} \frac{1}{R_L} + \frac{1}{R_f} & -\frac{1}{R_L} - \frac{1}{R_f} \\ -\frac{1}{R_L} - \frac{1}{R_f} & \frac{1}{R_L} + \frac{1}{R_f} \end{bmatrix} \begin{bmatrix} V_{x1} \\ V_{x2} \end{bmatrix} = 0 \qquad (5)$$

The equation has been split into three parts. The first is with the voltage sources. Since, the voltage source V_{in} and the capacitor voltage V_c are in branches with inductors, these branches are treated as current sources and the voltages are ignored. Only the capacitor voltage V_{cf} appears in the equations in the manner described above. In general, any voltage source (or capacitor voltage) will appear in the vector and the matrix can be written such that at the nodes where the positive terminal of the voltage source is incident, the element is -1 while if the negative terminal of the voltage source is incident, the element is +1. The second part of the equation consists of the inductor currents. They are feeding node V_{x1} and therefore are considered negative in the first equation while they are draining node V_{x2} and considered positive in the second equation. In general, all the inductors of the circuit are collected together in a list and if an inductor is feeding a node, the corresponding element is -1 while if it is draining a node, the element is +1. Finally, the last part of the equation contains the resistances. The node voltages are collected together in a list. In every equation, the diagonal elements of the matrix will contain the positive sum of all the admittances incident at that node. The off-diagonal elements are such that if a node is connected to the node corresponding to the diagonal element, the corresponding element will be the negative sum total of admittances of all the branches that connect these two nodes. If

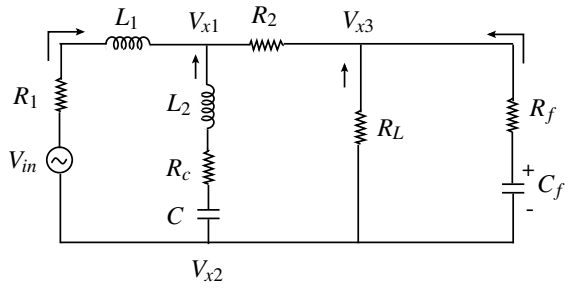

Figure 5: Sample circuit to describe admittance matrix

however, the nodes are not connected, the element will be zero.

The last concept can be better described with the circuit in Fig. 5. Another node V_{x3} has been introduced by placing the resistor R_2. For this circuit, the admittance matrix part can be written as follows:

$$\begin{bmatrix} \frac{1}{R_2} & 0 & -\frac{1}{R_2} \\ 0 & \frac{1}{R_L}+\frac{1}{R_f} & -\frac{1}{R_L}-\frac{1}{R_f} \\ -\frac{1}{R_2} & -\frac{1}{R_L}-\frac{1}{R_f} & \frac{1}{R_2}+\frac{1}{R_L}+\frac{1}{R_f} \end{bmatrix} \begin{bmatrix} V_{x1} \\ V_{x2} \\ V_{x3} \end{bmatrix}$$

Diagonal element (1, 1) contains all the admittances at node V_{x1} which in this case is only $\frac{1}{R_2}$ as the other two branches V_{in}, R_1, L_1 and R_c, L_2, C are current sources because of the inductors. The off-diagonal element (1, 2) is zero because node V_{x1} is not directly connected to node V_{x2} through a resistive branch and as before the branches with inductors don't count. The off-diagonal element (1, 3) is $-\frac{1}{R_2}$ since node V_{x1} is connected to the node V_{x3} by branch R_2 alone. On the other hand, diagonal element (2, 2) is $\frac{1}{R_L}+\frac{1}{R_f}$ as the node V_{x2} has branches with resistors R_2 and R_f incident on it. Node V_{x2} is not directly connected to node V_{x1} by a resistive branch and therefore off-diagonal element (2, 1) is zero. For off-diagonal element (2, 3), node V_{x2} and node V_{x3} are connected by two branches with resistors R_L and R_f respectively and therefore element (2, 3) is the negative sum $-\frac{1}{R_L}-\frac{1}{R_f}$. The last row of the matrix is left to the reader.

4 Conclusions

This paper has described how for a circuit, the matrix equations for loop analysis and nodal analysis can be generated. Using sample circuits, the algorithm has been described on how

passive circuits will be represented with respect to the loop and nodal equations. The equations that are generated will need to be solved. In the case of loop analysis, the equation is a differential equation in case the circuit has inductors. Therefore, the loop analysis will need an ordinary differential equation solver. On the other hand, if the circuit has no inductors, the equations will be simple algebraic equations. For nodal analysis, the equations are always simple algebraic equations. The method of solving equations will be described in a future short paper.